

Patent claims:

1. A polymer transistor arrangement
 - having a polymer transistor which is formed in
5 and/or on a substrate and has
 - a first source/drain region;
 - a second source/drain region;
 - a channel region between the first and second
source/drain regions;
 - 10 ◦ a gate region;
 - a gate-insulating layer between channel region
and gate region;
 - having a drive circuit which is set up in such a
way that it provides the source/drain regions
15 and the gate region with electrical potentials
such that the junction between at least one of
the source/drain regions and the channel region
can be operated as a diode.
- 20 2. The polymer transistor arrangement as claimed in
claim 1,
in which the drive circuit is set up in such a way
that it provides the source/drain regions and the
gate region with electrical potentials such that
25 the junction between one of the two source/drain
regions and the channel region is connected as a
reverse-biased diode.
3. The polymer transistor arrangement as claimed in
30 claim 1 or 2,
in which the channel region and the source/drain
regions are produced from a material such that the
junction between one of the source/drain regions
and the channel region is
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 - a Schottky junction;
 - an in junction;
 - an ip junction; or
 - a pn junction.

4. The polymer transistor arrangement as claimed in one of claims 1 to 3,
in which the drive circuit is set up in such a way
5 that the magnitude of the gate voltage is greater than the magnitude of the voltage between the source/drain regions.
5. The polymer transistor arrangement as claimed in
10 one of claims 1 to 4,
in which the junctions between a respective one of the source/drain regions and the channel region are formed geometrically asymmetrically with respect to one another.
6. The polymer transistor arrangement as claimed in
15 one of claims 1 to 5,
in which one of the source/drain regions is formed at least partially on the channel region and the
20 other source/drain region is formed at least partially below the channel region.
7. An integrated circuit arrangement
having at least one polymer transistor arrangement
25 as claimed in one of claims 1 to 6.
8. The integrated circuit arrangement as claimed in claim 7,
set up as a reference voltage circuit.
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9. The integrated circuit arrangement as claimed in claim 7 or 8,
set up as a temperature-compensated reference voltage circuit.
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10. The integrated circuit arrangement as claimed in one of claims 7 to 9,
set up as a current source.

11. The integrated circuit arrangement as claimed in claim 7,
set up as a voltage control circuit.

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12. A method for producing a polymer transistor arrangement,
in which

- a polymer transistor is formed in and/or on a substrate by
 - o a first source/drain region being formed;
 - o a second source/drain region being formed;
 - o a channel region being formed between the first and second source/drain regions;
 - o a gate region being formed;
 - o a gate-insulating layer being formed between channel region and gate region;

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a drive circuit being formed, which is set up in such a way that it provides the source/drain regions and the gate region with electrical potentials such that the junction between at least one of the source/drain regions and the channel region is operated as a diode.